KINGS COLLEGE OF ENGINEERING AUTONOMOUS

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NAAC Accredited Institution

Department of Training and Placement

Academic Year 2024 - 2025

A report on Virtual career awareness session on "VLSI Design Verification"

Our department organized an awareness session on VLSI design verification through virtual mode on 21.11.2024 at respective department smart classroom, aimed to educate participants about the importance and methodologies of verifying Very Large Scale Integration (VLSI) designs. VLSI design verification is a critical step in the VLSI design flow, ensuring that the designed chip meets the required specifications and functions correctly.

The webinar was started with a welcome note by Dr. B. Suresh Babu, ASP/TPO, Department of Training and Placement (Management Studies).

Key Topics Covered

- VLSI Design Flow: The session likely covered the various stages involved in VLSI design, including idea conception, specification, design architecture, RTL coding, RTL verification, synthesis, and fabrication.
- Verification Methodologies: Participants were probably introduced to different verification methodologies, such as simulation-based verification, formal verification, and emulation-based verification.
- Importance of Verification: The session highlighted the significance of verification in ensuring the functionality, performance, and reliability of VLSI designs.
- Challenges in VLSI Verification: Participants may have discussed the challenges faced during VLSI verification, including increasing design complexity, shrinking geometries, and higher frequencies.

Key Takeaways

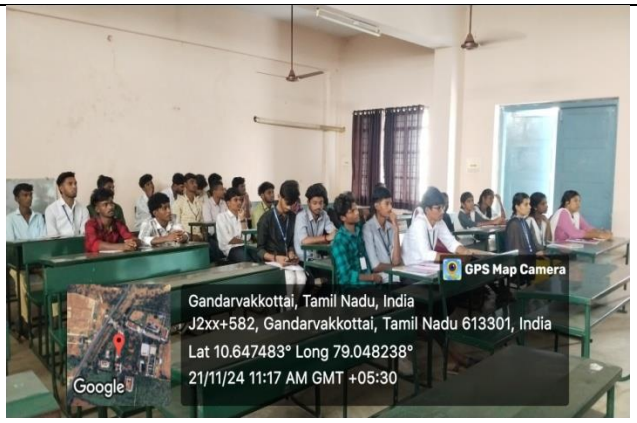
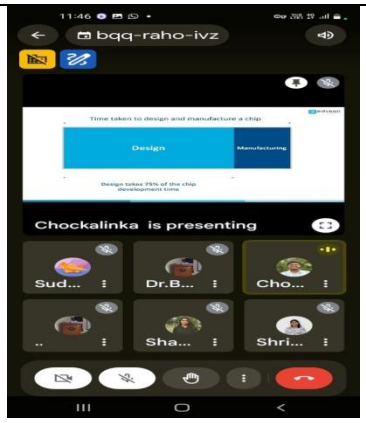
- VLSI design verification is crucial to ensure the designed chip meets the required specifications and functions correctly.
- Various verification methodologies are used in VLSI design, including simulation-based verification, formal verification, and emulation-based verification.
- Verification is an ongoing challenge in VLSI design due to increasing design complexity and shrinking geometries.

Benefits of VLSI Design Verification

- Improved Design Quality: Verification ensures that the designed chip meets the required specifications and functions correctly.
- Reduced Design Cycle Time: Effective verification methodologies can help reduce the design cycle time and get the product to market faster.
- Cost Savings: Verification can help detect and fix errors early in the design cycle, reducing the cost of redesign and re-fabrication.

Beneficiaries:

Around 85 final year students of ECE and EEE were benefited from the programme.

	
A view of participants	**Screen shot of the webinar**

TPO **VP/Head-T&P** **Principal**